

cont
BJ

formed deep. On this occasion, an impurity diffused layer 106 is provided in the substrate potential take-out region by implanting the ions of the same conductivity as that of the substrate. In the case of, e.g., an n-channel MOS, the ions, i.e., n-type impurities such as phosphorus are implanted into the device region, and the ions, viz., p-type impurities such as boron are implanted into the substrate potential take-out region.---

See the attached Appendix for the changes made to effect the above paragraph.

IN THE CLAIMS:

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Please cancel claims 5 and 12 without prejudice.

Please enter the following amended claims:

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1. (Amended) A semiconductor device comprising:
 - a semiconductor substrate;
 - a MOSFET formed on the substrate;
 - a first interconnection connected to a gate of the MOSFET, wherein said first interconnection constitutes a signal input pad for receiving an input signal for the MOSFET;
 - a high concentration impurity diffused region located under the first interconnection and at a surface part of the semiconductor substrate;
 - a second interconnection connected to the high concentration impurity diffused region; and
 - a low resistance layer provided on the upper surface of the high concentration impurity diffused region.

7. (Amended) A semiconductor device comprising:

- a semiconductor substrate;
- a MOSFET formed on the substrate;
- a first interconnection connected to a gate of the MOSFET, wherein said first interconnection constitutes a signal input pad for receiving an input signal for the MOSFET;
- a high concentration impurity diffused region located below the first interconnection and at a surface part of the semiconductor substrate;
- a second interconnection connected to the high concentration impurity diffused region;
- a low resistance layer provided on the upper surface of the high concentration impurity diffused region; and
- a polysilicon layer provided below the first interconnection, said polysilicon layer being connected to the second interconnection.

See the attached Appendix for the changes made to effect the above claims.

. Please add the following new claims:

---16. (New) The semiconductor device according to claim 1, wherein said first interconnection and said second interconnection are not connected.---

---17. (New) The semiconductor device according to claim 7, wherein said first interconnection and said second interconnection are not connected.---